PTO/SB/21 (09-06)

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NAME OF THE OWNER OWNER OF THE OWNER		Application Number	10/708,256	
TRANSMITTAL FORM  (to be used for all correspondence after initial filing)		Filing Date	02/19/2004	
		First Named Inventor	Hsin-Shih Wang	
		Art Unit	2825	
		Examiner Name	SIEK, VUTHE	
Total Number of Pages in This Submission	9	Attorney Docket Number	FTCP0031USA	

Total Nullibe	t of Fages in This Suphinssion	<del></del>	Attorney Docket Number	FICH	003103A			
		ENC	LOSURES (Check	all that apply	<i>(</i> )			
Fee Tr	ansmittal Form		Drawing(s)		After Allowance Communication to TC  Appeal Communication to Board			
Fee Attached  Amendment/Reply  After Final  Affidavits/declaration(s)  Extension of Time Request  Express Abandonment Request  Information Disclosure Statement  Certified Copy of Priority Document(s)  Reply to Missing Parts/ Incomplete Application  Reply to Missing Parts  under 37 CFR 1.52 or 1.53			Petition Petition to Convert to a Provisional Application Power of Attorney, Revoc Change of Correspondence Terminal Disclaimer Request for Refund CD, Number of CD(s) Landscape Table or	ce Address	of Appeals and Interferences  Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)  Proprietary Information  Status Letter Other Enclosure(s) (please Identify below):  1.A copy of front page of patent 2.A copy of filing receipt 3.A copy of fee transmittal 4.PTO/SB/44			
		Reque			of Office Mistake  Certificate  OR AGENT APR 9 2 2007			
	SIGNA	TURE C	OF APPLICANT, AT	TORNEY, C	OR AGENT APR OF B			
Firm Name	North America Intelle	ctual Pro	perty Corporation		of Correction			
Signature	aluntos Ho	re			•			
Printed name	Winston Hsu				•			
Date	MAR 28 2007			Reg. No.	41,526			
	CERTIFICATE OF TRANSMISSION/MAILING							

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PTO/SB/17 (02-07)

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Effective on 12		Complete if Known			
Fees pursuant to the Consolidated Appl		Application Number	10/708,256		
FEE TRAN	ISMITTAL	Filing Date	02/19/2004	<u> </u>	
For FY	2005	First Named Inventor	Hsin-Shih Wang		
Applicant claims small entity status. See 37 CFR 1.27  TOTAL AMOUNT OF PAYMENT (\$) 0.00		Examiner Name	SIEK, VUTHE		
		Art Unit	2825		
		Attorney Docket No.	FTCP0031USA		
METHOD OF PAYMENT (chec	k all that apply)				

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information and authorization		· ·					
FEE CALCULATION							
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Design	200	- 100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	-
Provisional	200	100	0	0	0	0	
2. EXCESS CLAIM F Fee Description Each claim over 20 ( Each independent claim Multiple dependent	EES (including R aim over 3 ( claims	Reissues) (including Reissu	es)	•		Fee (\$) 50 200 360	Small Entity Fee (\$) 25 100 180 ependent Claims
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3. APPLICATION SIZ  If the specification and listings under 37 C sheets or fraction t Total Sheets	E FEE d drawings ( CFR 1.52(e)	exceed 100 sheets), the application	s of paper size fee di	ue is \$250 (\$)	125 for small	l entity) for e	<del>-</del>
- 100 =  4. OTHER FEE(S)  Non-English Specification  Other (e.g., late filing)		•	`	round <b>up</b> to a v count)	vhole number)	) X	=

SUBMITTED BY			
Signature	Calanton Hora	Registration No. (Attorney/Agent) 41,526	Telephone 3027291562
Name (Print/Type)	Winston Hsu		Date MAR 28 2007

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### IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Serial No.: 10/708,256 Filing Date: 02/19/2004

Inventor : Hsin-Shih Wang

Docket No.: FTCP0031USA

Title: METHOD OF FABRICATING AN INTEGRATED CIRCUIT THROUGH
UTILIZING METAL LAYERS TO PROGRAM RANDOMLY POSITIONED BASIC
UNITS

To:

Commissioner for Patents

P.O. BOX 1450

Alexandria, VA 22313-1450

Subject: Request for Certificate of Correction of Office

Mistake

The above-identified patent was issued on 02/27/2007. The applicant found that the invention title listed on the front page of the patent is not correct (Attachment 1). Documents on record indicate this as an Office mistake of consequence.

The applicant hereby requests that a Certificate of Correction be issued under 37 CFR 1.322 to correct the invention title from "METHOD OF FABRICATING AND INTEGRATED CIRCUIT THROUGH UTILIZING METAL LAYERS TO PROGRAM RANDOMLY POSITIONED BASIC UNITS" to "METHOD OF FABRICATING AN INTEGRATED CIRCUIT THROUGH UTILIZING METAL LAYERS TO PROGRAM RANDOMLY POSITIONED BASIC UNITS" as correctly listed on the Filing Receipt dated May 14, 2004 (Attachment 2) and the Fee Transmittal submitted on Jan. 23, 2007 (Attachment 3).

Respectfully submitted,

Wintentan Lan Date: MAR 28

Winston Hsu, Patent Agent No. 41,526

P.O. BOX 506, Merrifield, VA 22116, U.S.A.

Voice Mail: 302-729-1562\_\_\_\_

Facsimile: 806-498-6673

e-mail: winstonhsu@naipo.com

Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)

Please correct the invention title from "METHOD OF FABRICATING AND INTEGRATED CIRCUIT THROUGH UTILIZING METAL LAYERS TO PROGRAM RANDOMLY POSITIONED BASIC UNITS" to "METHOD OF FABRICATING AN INTEGRATED CIRCUIT THROUGH UTILIZING METAL LAYERS TO PROGRAM RANDOMLY POSITIONED BASIC UNITS".



(12) United States Patent

US 7,185,307 B2 (10) Patent No.:

Wang

(45) Date of Patent: Feb. 27, 2007

METHOD OF FABRICATING AND INTEGRATED CIRCUIT THROUGH RANDOMLY POSITIONED BASIC UNITS

UTILIZING METAL LAYERS TO PROGRAM

(75) Inventor: Hsin-Shih Wang, Fremont, CA (US)

Assignee: Faraday Technology Corp., Hsin-Chu (TW)

Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 390 days.

Appl. No.: 10/708,256 (21)

(22)Feb. 19, 2004 Filed:

(65)**Prior Publication Data** 

US 2005/0186714 A1 Aug. 25, 2005

(51) Int. Cl. G06F 17/50 (2006.01)

(52) U.S. Cl. ...... 716/17; 716/1

Field of Classification Search ...... 716/1, (58) 716/8, 11, 16–17; 438/128–129; 257/691 See application file for complete search history.

References Cited (56)

### **U.S. PATENT DOCUMENTS**

6,445,065 B1 *	9/2002	Gheewala et al 257/691
6,902,957 B2 *	6/2005	Wang et al 438/128
2003/0140080 A1 *	7/2003	Friend et al 708/700

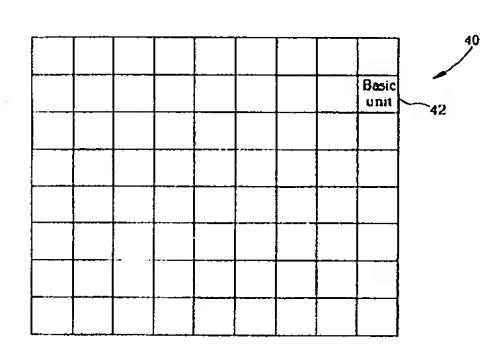
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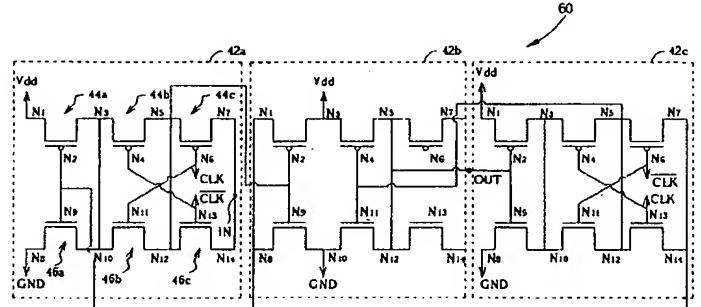
Primary Examiner—Vuthe Siek (74) Attorney, Agent, or Firm-Winston Hsu

#### **ABSTRACT** (57)

A method of fabricating an integrated circuit. The integrated circuit has a semiconductor body. The method includes forming a plurality of basic units with the same component characteristic on the semiconductor body, and forming at least a layout layer to program the basic units for building a clocked logic circuit and a non-clocked logic circuit without placing restrictions on positions of the clocked logic circuit and the non-clocked logic circuit on the semiconductor body.

### 17 Claims, 13 Drawing Sheets





Page 1 of 2

MAR 2 9 2007 BY HATES

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1	APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY.DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS	
	10/708.256	02/19/2004	2819	446	FTCP0031USA	13	22	4	

**CONFIRMATION NO. 2255** 

027765 NAIPO (NORTH AMERICA INTERNATIONAL PATENT OFFICE) P.O. BOX 506 MERRIFIELD, VA 22116



Date Mailed: 05/14/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

Hsin-Shih Wang, Fremont, CA;

Domestic Priority data as claimed by applicant

Foreign Applications

If Required, Foreign Filing License Granted: 05/13/2004

**Projected Publication Date: 08/25/2005** 

Non-Publication Request: No

Early Publication Request: No

\*\* SMALL ENTITY \*\*

Title

METHOD OF FABRICATING AN INTEGRATED CIRCUIT THROUGH UTILIZING METAL LAYERS TO PROGRAM RANDOMLY POSITIONED BASIC UNITS

**Preliminary Class** 

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Attachment 3

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		PRO THAT		Brenda (in			(Signature)
		O THAI		01/23/2007			(Date)
APPLICATION NO	FILING DATE		FIRST NAMED INVENT	OR	ATTORN	EY DOCKET NO	CONFIRMATION NO.
10/708,256	02/19/2004		Hsin-Shih Wang		FTC	CP0031USA	2255
TITLE OF INVENTION	INICI NOU OF FA	BRICATING AN INT SITIONED BASIC U		IT THROUGH L	ITILIZING	METAL LAYER	S TO PROGRAM
APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DU	JE PREV. PAID ISS	UE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$0	A	\$1700	03/14/2007
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3. ASSIGNEE NAME A			·-	• • •			
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Faraday Techno	ology Corp.			oad 3, Science	-Based I	ndustrial Park,	Hsin-Chu City,
· ·		categories (will not be pr	Taiwan, R.O.C. inted on the patent):	☐ Individual ☑	Corporation	or other private gro	up entity Government
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Issue Fee			A check is enclose			, <b>P</b>	,
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an application Confident submitting the completed this form and/or suggestion	iality is governed by 35 application form to the ons for reducing this builtginia 22313-1450. DC	U.S.C. 122 and 37 CFR USPTO. Time will vary rden, should be sent to the	1.14. This collection is depending upon the in Chief Information Off	estimated to take 12 dividual case. Any ficer, U.S. Patent an	2 minutes to comments of Trademark	complete, including in the amount of time k Office, U.S. Depa	by the USPTO to process) g gathering, preparing, and ne you require to complete rtment of Commerce, P.O. for Patents, P.O. Box 1450,
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(Also Form PTO-1050)

## UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

	Page1 of1
PATENT NO. : 7,185,307 B2	
APPLICATION NO.: 10/708,256	
ISSUE DATE : Feb. 27, 2007	· · ·
INVENTOR(S) : Hsin-Shih Wang	
It is certified that an error appears or errors appear in the above-identified patent and the is hereby corrected as shown below:	at said Letters Patent
On the title page item (54), and col. 1, line 1, change	
"METHOD OF FABRICATING AND INTEGRATED CIRCUIT THROUGH UTILIZING MET TO PROGRAM RANDOMLY POSITIONED BASIC UNITS"  to	TAL LAYERS
METHOD OF FABRICATING AN INTEGRATED CIRCUIT THROUGH UTILIZING MET. TO PROGRAM RANDOMLY POSITIONED BASIC UNITS	AL LAYERS
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